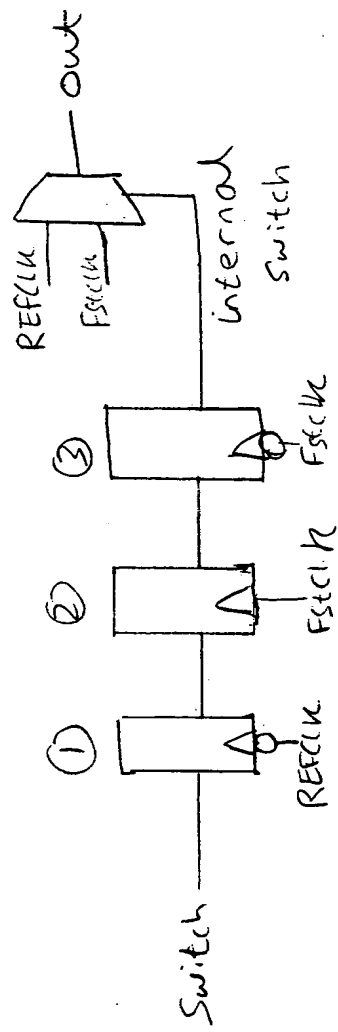
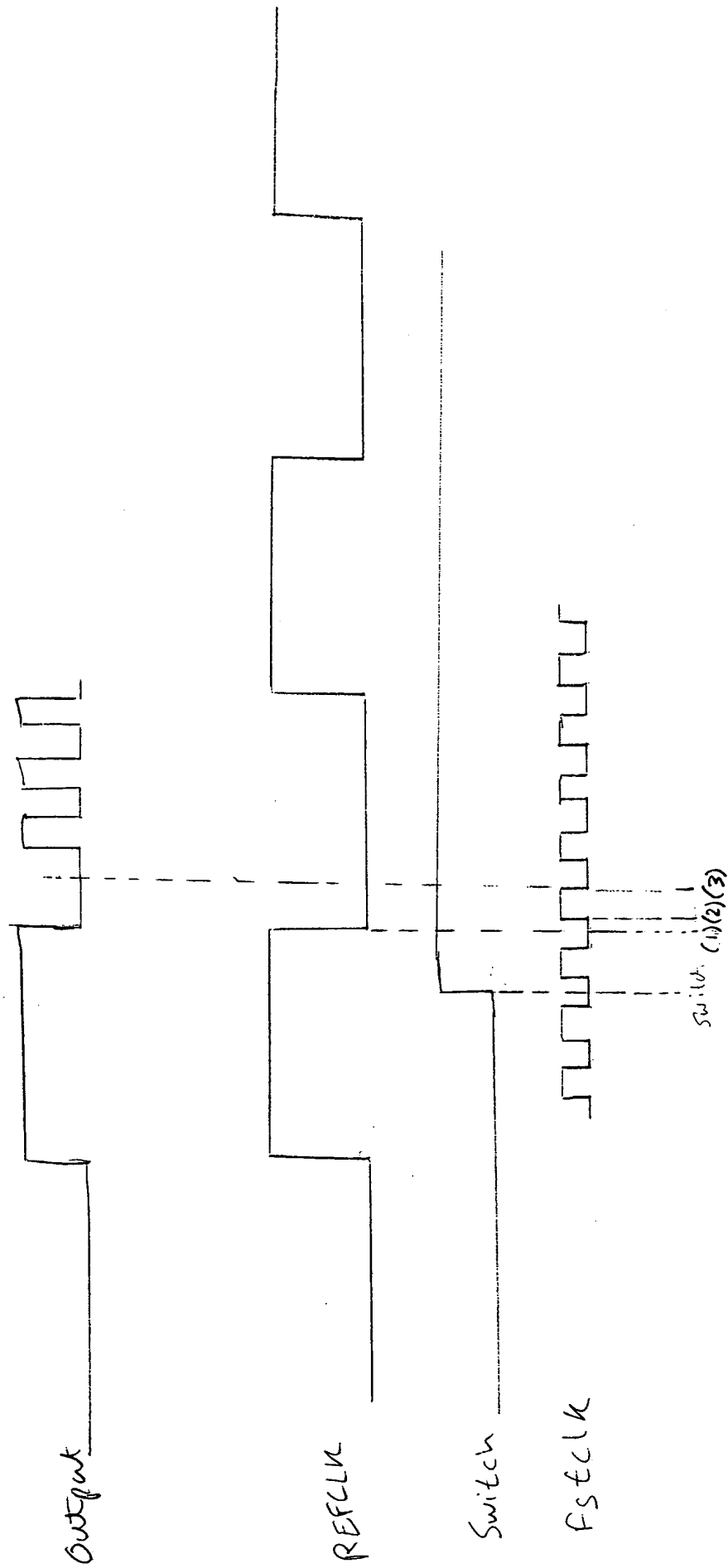


Prior art

Figure 1





Prior art

Figure 2

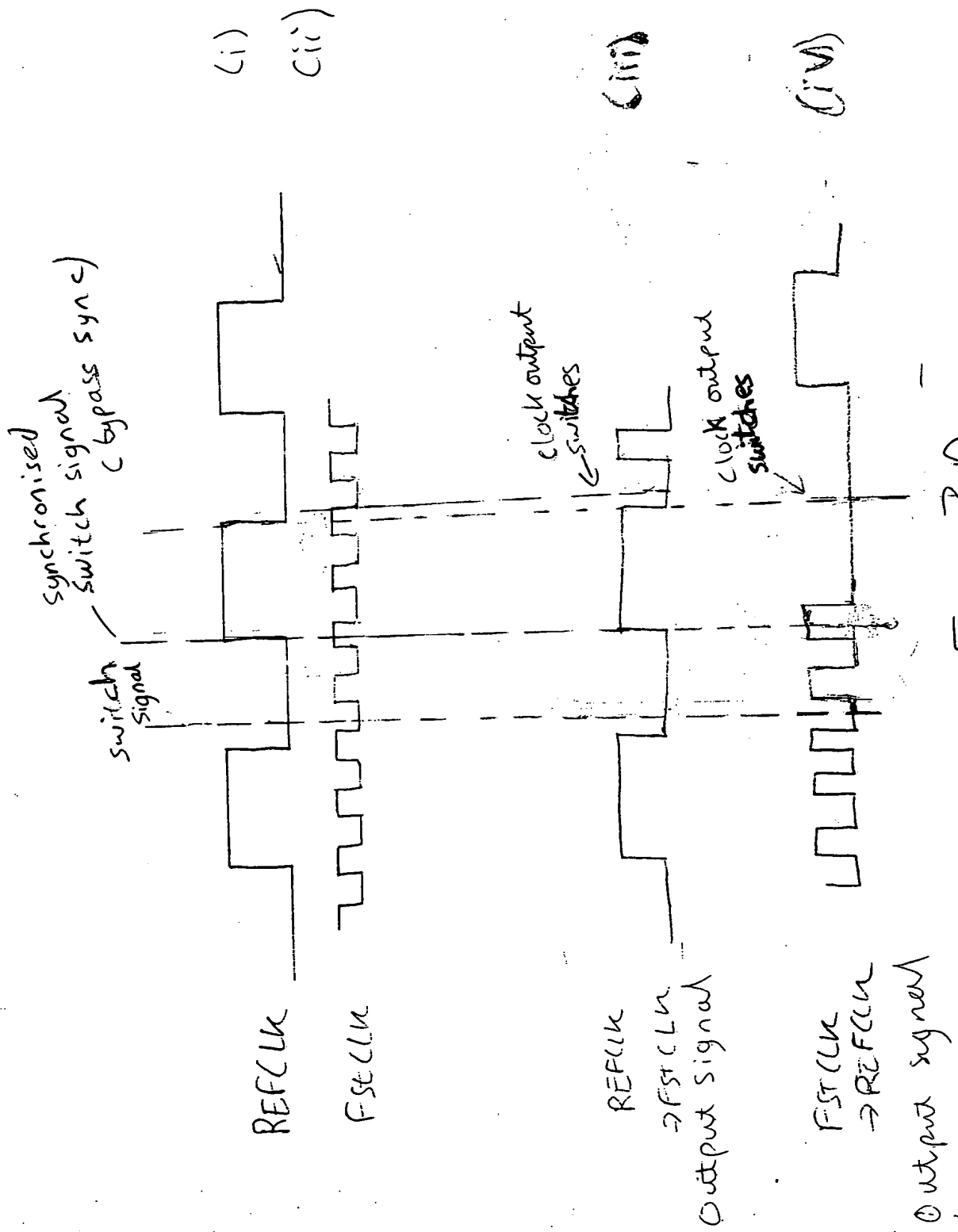


Figure 3 A

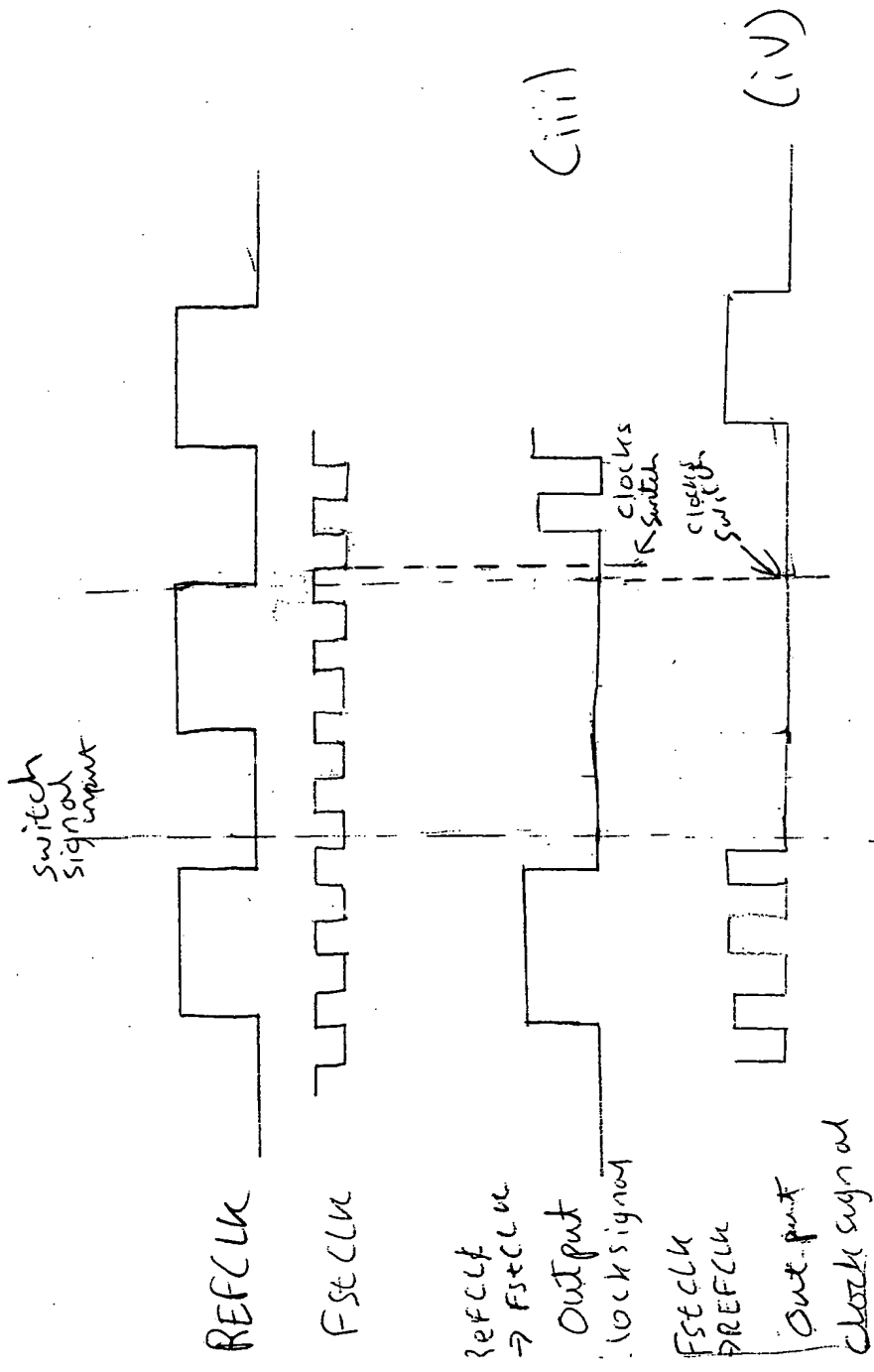


Figure 3B

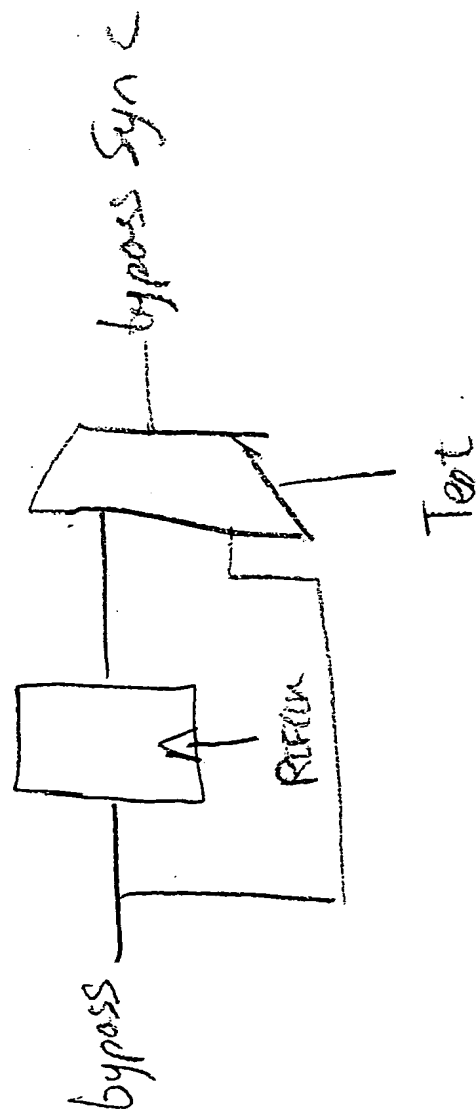
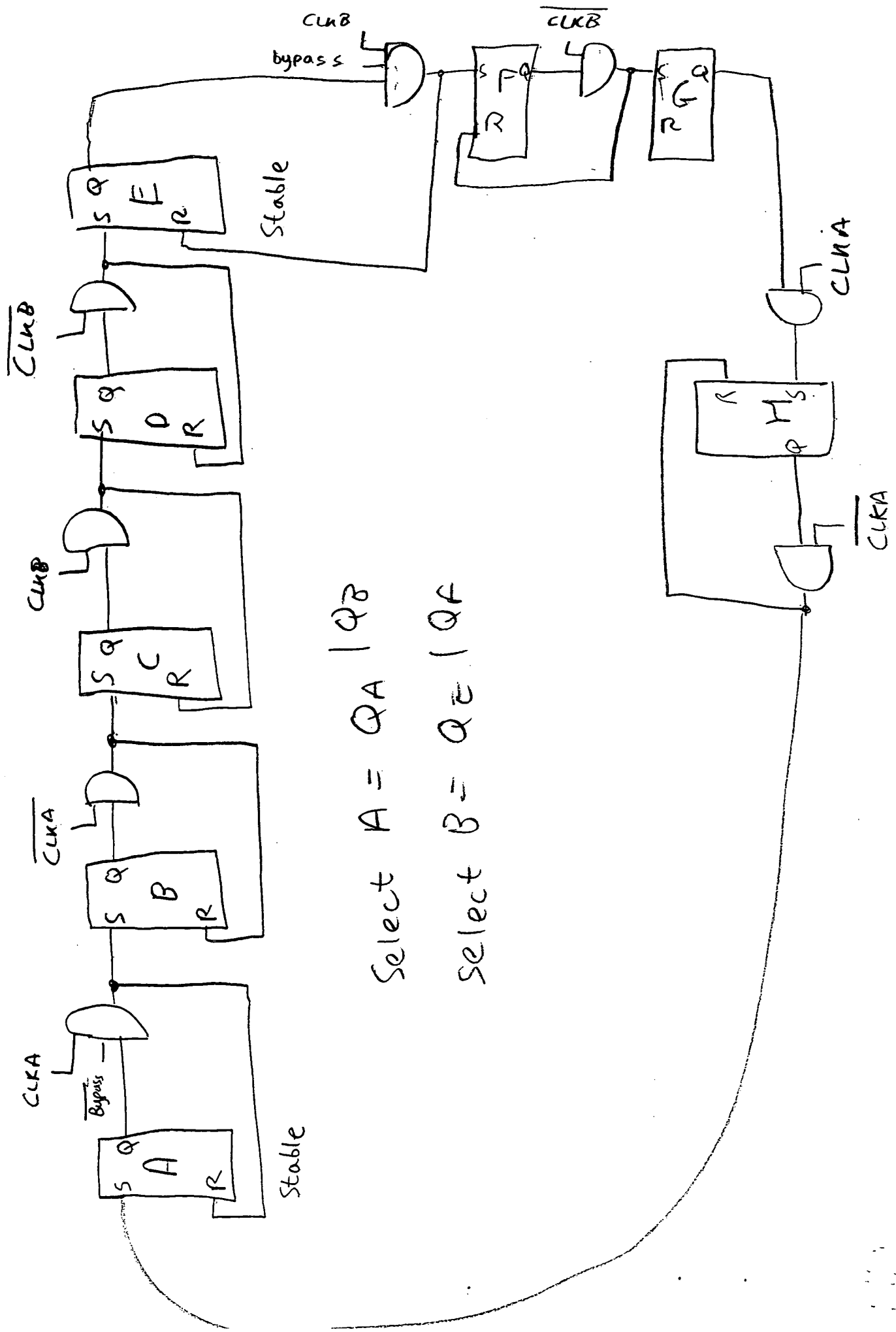


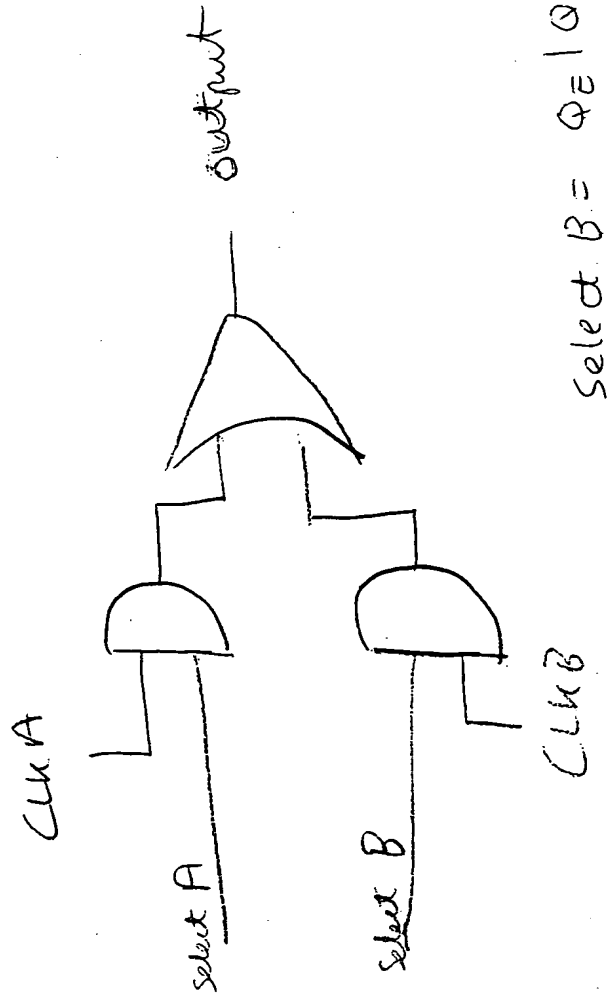
Figure 4



Select  $A = Q_A \mid Q_B$   
 Select  $B = Q_C \mid Q_D$

Figure 1

$$\text{Select } A = Q_A \mid Q_B$$



$$\text{Select } B = Q_E \mid Q_F$$

Figure 6

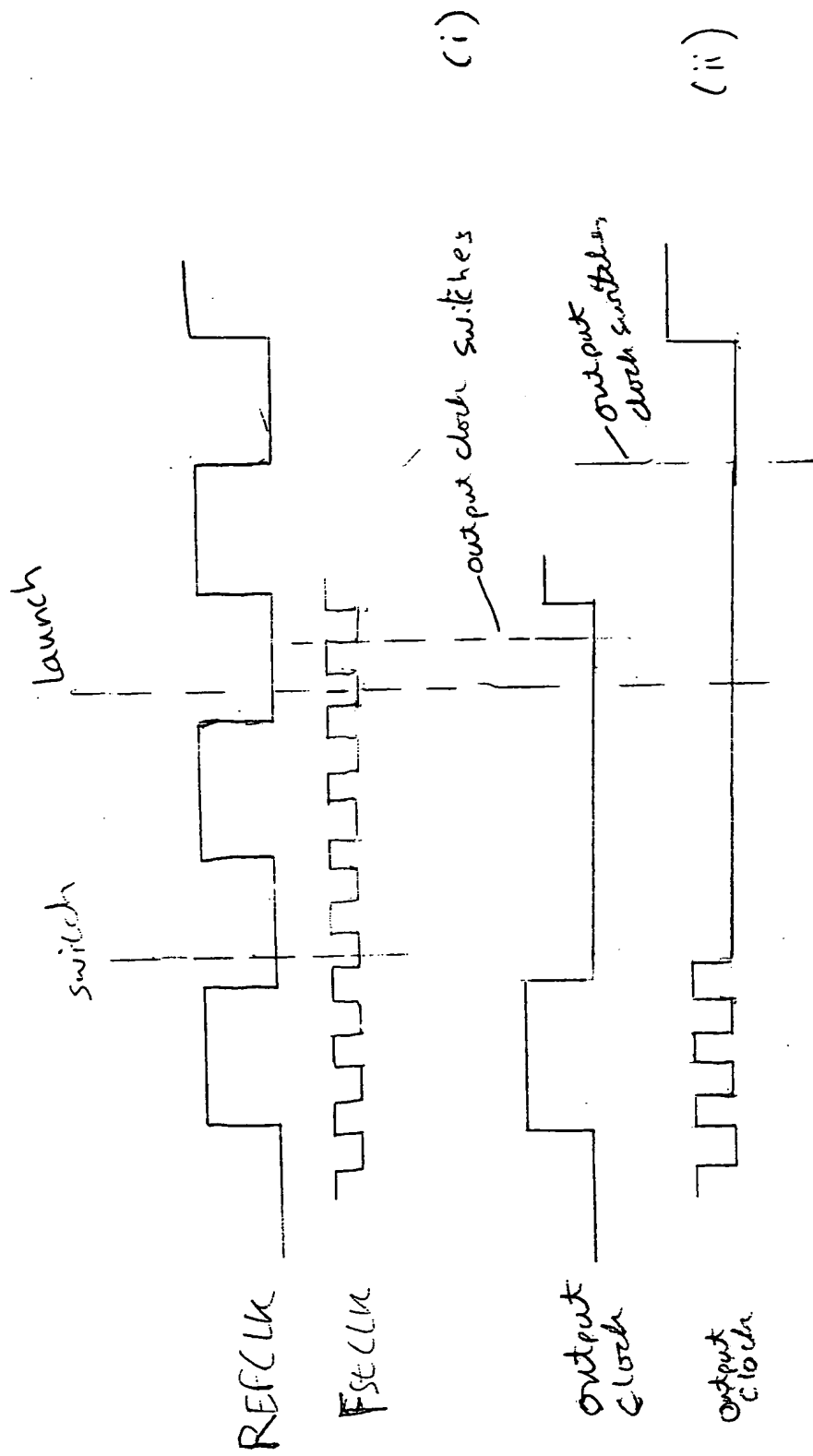


Figure 7

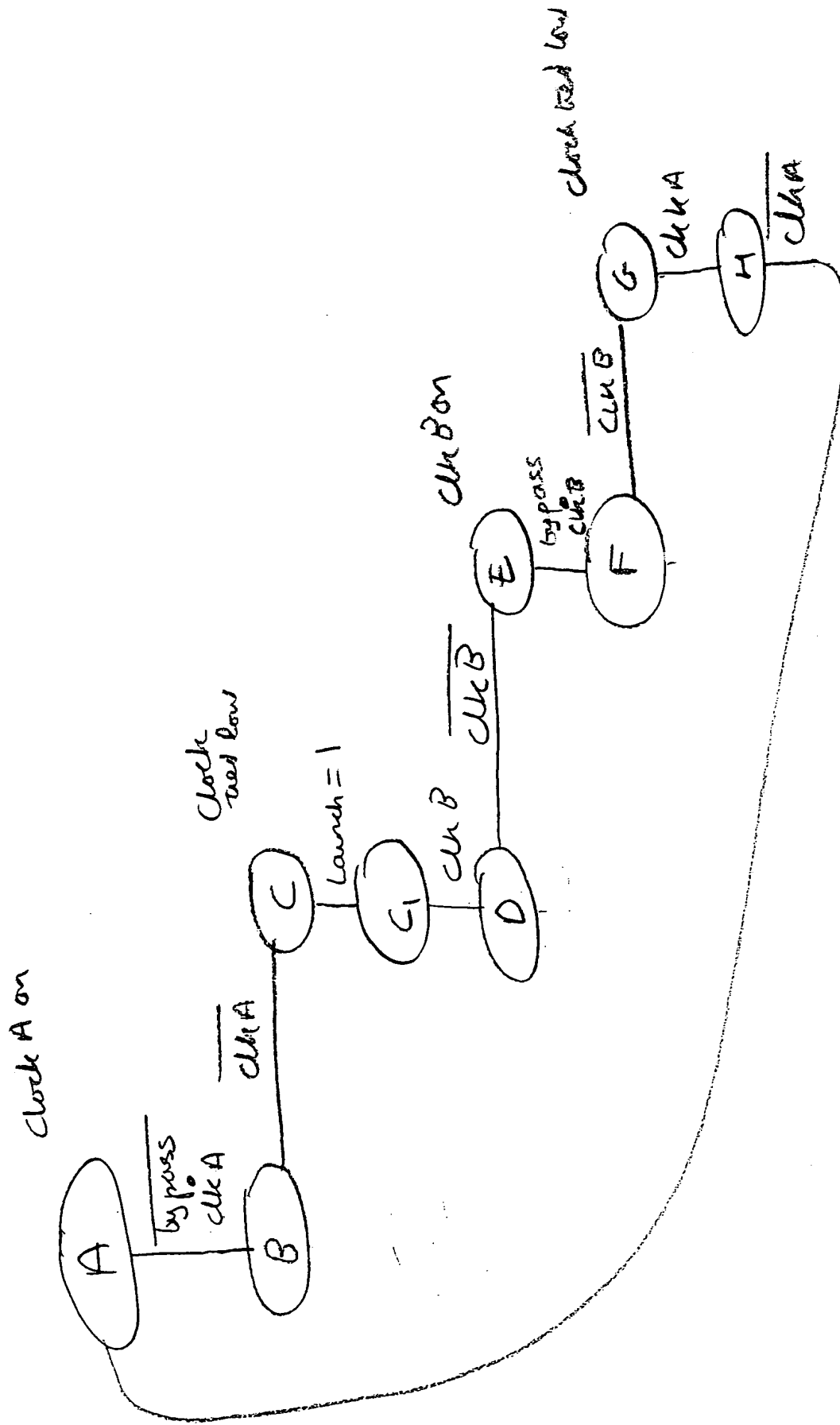


Figure 8

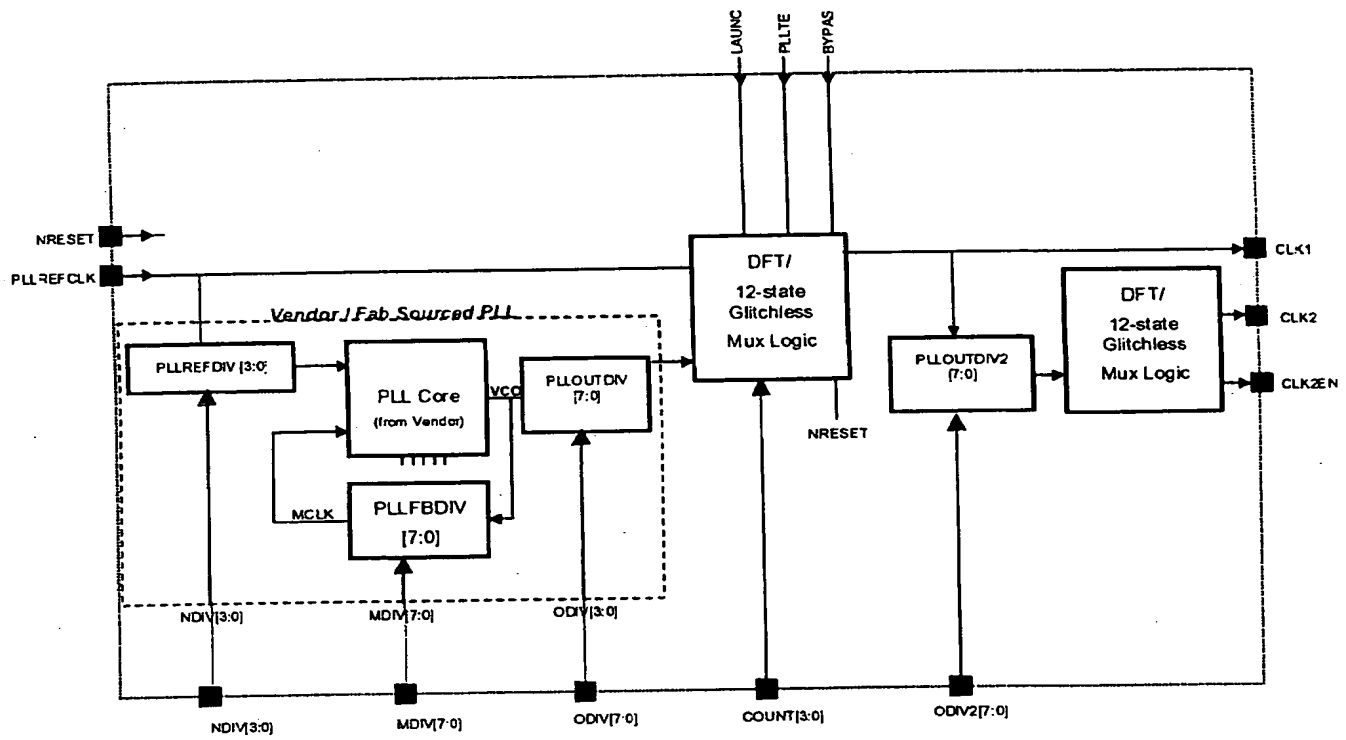


Figure 9

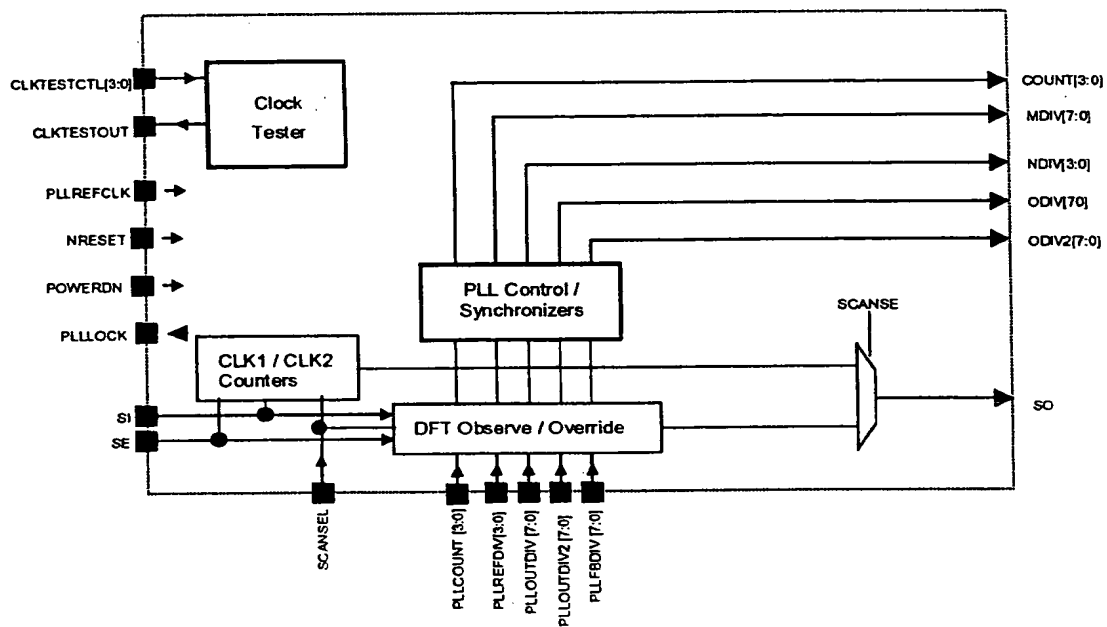


Figure 10.

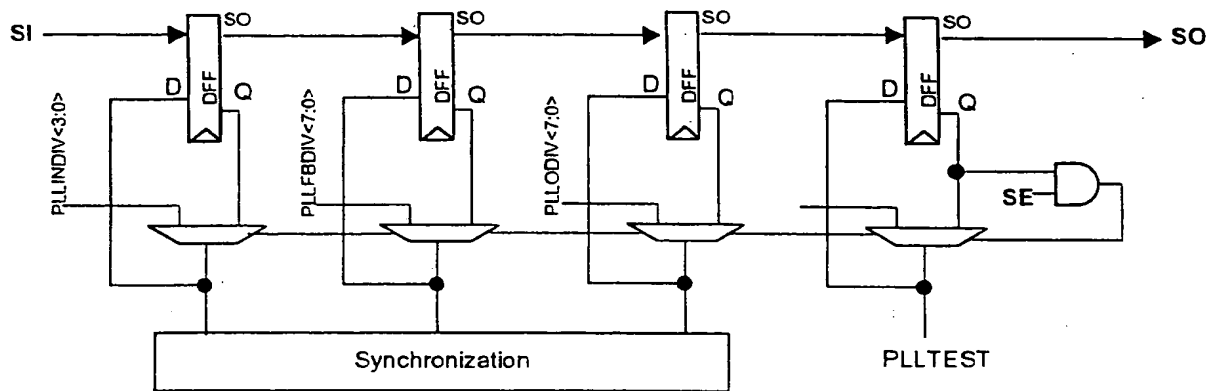
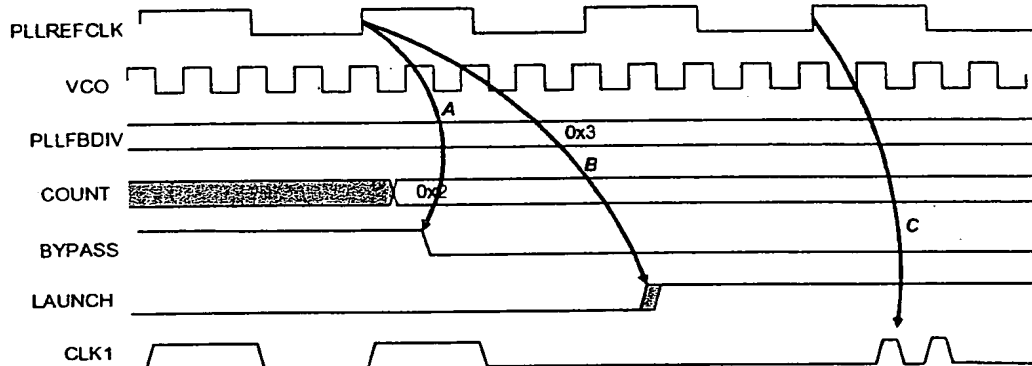


Figure 11



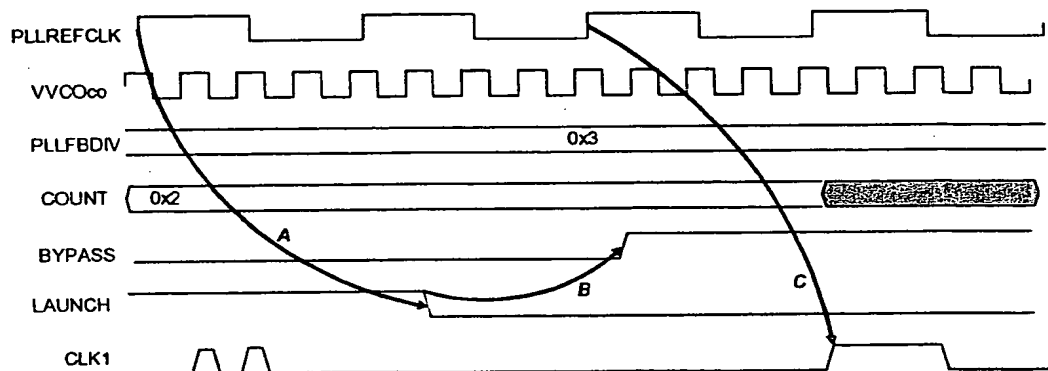
**A:** BYPASS toggles from tester pad after a rising edge of reference clock. Arrival must be within one PLLREFCLK, and not necessarily within one phase.

**B:** The asserting edge of the LAUNCH signal enables the generation of CLK1 in the VCO domain. LAUNCH must arrive at least one PLLREFCLK cycle after BYPASS toggles. Similar to BYPASS, LAUNCH arrives within one PLLREFCLK.

**C:** CLK1, in the VCO domain, is generated within the next PLLREFCLK cycle after LAUNCH is received. The start of CLK1 should begin within one PLLREFCLK cycle. The alignment to the PLLREFCLK phase is not specifically required.

Notes: It is illegal for BYPASS or LAUNCH to re-toggle before the appropriate number of CLK1 pulses is generated (except for indefinite mode). All PLL input control must have proper slew rate to guarantee the behaviour described.

Figure 12



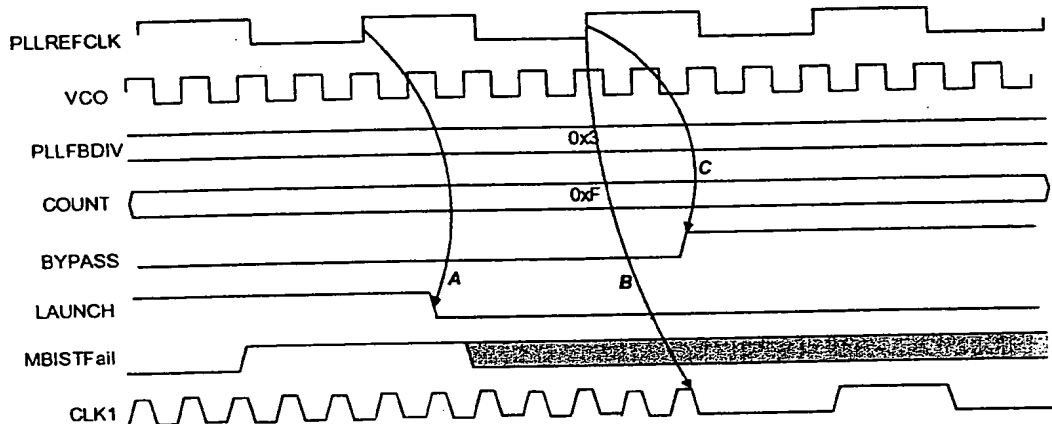
**A:** LAUNCH is de-asserted one PLLREFCLK cycle after the required number of CLK1 pulses, in the VCO domain, have been generated. This de-assertion of LAUNCH will vary as a function of COUNT, PLLFBDIV, design implementation, and is the responsibility of a DFT Engineer to generate a sufficient number of cycles in the test program to guarantee behaviour.

**B:** BYPASS must be asserted at least one PLLREFCLK cycle after LAUNCH de-assertion.

**C:** CLK1 will track the PLLREFCLK in the cycle following BYPASS assertion.

Notes: If design implementation requires additional cycles to transition (eg: C: requires a second PLLREFCLK before CLK1=PLLREFCLK), this may be allowed. Any change in CLK1 behaviour as a function of BYPASS must be 100% deterministic with respect to the cycle counts specified.

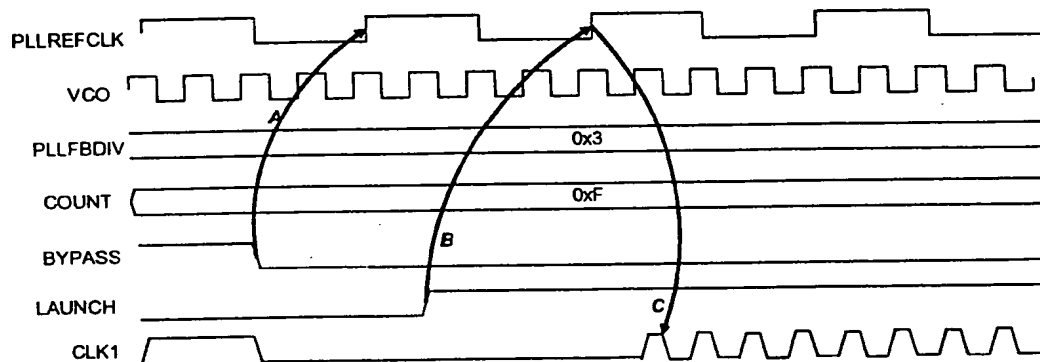
Figure 13



- A:** LAUNCH is de-asserted by the tester one PLLREFCLK cycle after MBIST failure is detected.
- B:** CLK1, in the VCO domain, should terminate in the next PLLREFCLK cycle after LAUNCH de-assertion. Because the MBIST controller is in a stalled state, the number of CLK1 pulses delivered is not of concern; however, the exact PLLREFCLK cycle must be known.
- C:** BYPASS may be asserted as early as the first cycle following LAUNCH de-assertion or in any later PLLREFCLK cycle.

Notes: MBISTFail is not a PLL specified signal but is shown here as trigger mechanism for test action. Once the tester has de-asserted LAUNCH, MBISTFail is used as a datalog output.

Figure 14



**A:** The de-assertion of BYPASS, masks all subsequent CLK1 pulses, in the PLLREFCLK domain.

**B:** The assertion of LAUNCH enables CLK1 pulses to be generated in the VCO domain in subsequent PLLREFCLK cycles.

**C:** CLK1 generation in the VCO domain begins less than two VCO pulses after the PLLREFCLK rising edge.

Notes: Although similar to functional mode in switching between VCO and PLLREFCLK clock domains, the deterministic behavior of the LAUNCH signal is required for generation of tester vector sets. Example: A PLLREFCLK, creating event C, will strobe for an MBIST failure with expectations that at least one CLK1 pulse has been generated (strobe in the later half of PLLREFCLK cycle).

Figure 15.